

## CLAIM AMENDMENTS

1           1. (currently amended) A method for fine  
2       synchronization of a digital telecommunication receiver, comprising  
3       a code tracking process for maintaining fine alignment between an  
4       incoming spread spectrum signal and a locally generated code, said  
5       method comprising: [[-]]

6           storing a plurality of consecutive samples [(E-1, E, M,  
7       L, Li-1)] of said incoming spread spectrum signal in a delay line  
8       [(56)]; [[-]]

9           determining by interpolation between consecutive samples  
10       of said incoming spread spectrum signal, by means of a first  
11       [(26)] digitally controlled interpolator, an interpolated early  
12       sample [(e)] anticipating an optimal sampling time instant; [[-]]

13           determining by interpolation between consecutive samples  
14       of said incoming spread spectrum signal, by means of a second  
15       [(24)] digitally controlled interpolator, an interpolated middle  
16       sample [(m)] corresponding to said optimal sampling time instant;  
17       [[-]]

18           determining by interpolation between consecutive samples  
19       of said incoming spread spectrum signal, by means of a third  
20       [(28)] digitally controlled interpolator, an interpolated late  
21       sample [(1)] delayed with respect to said optimal sampling time  
22       instant; [[-]]

23           calculating an error signal  $[(4)]$  as the difference  
24   between the energy of the symbols computed from said interpolated  
25   early  $[(e)]$  and late  $[(1)]$  samples;  $[-]$  and  
26           generating, from said error signal  $[(a)]$ , a control  
27   signal  $[(S_{out})]$  for controlling the interpolation phase of said  
28   second digitally controlled interpolator  $[(24)]$ ; ~~characterised in~~  
29   ~~that said~~  
30   wherein the step of generating a control signal  $[(S_{out})]$   
31   comprises:  $[-]$   
32           extracting the sign of said error signal  $[(\xi)]$ ;  $[-]$   
33           accumulating said sign of said error signal  $[(\xi)]$  for  
34   the generation of an intermediate control signal  $[(S_M)]$ ;  $[-]$   
35           calculating the absolute value  $[(|\xi|)]$  of said error  
36   signal  $[(\xi)]$  at a time instant  $n$ ;  $[-]$   
37           comparing said absolute value  $[(|\xi(n)|)]$  of said error  
38   signal  $[(\xi)]$  at said time instant  $n$  with the absolute value  
39    $[(|\xi(n-1)|)]$  of said error signal  $[(\xi)]$  at a previous time  
40   instant  $n-1$ ;  $[-]$  and  
41           updating said control signal  $[(S_{out})]$  to the value of  
42   said intermediate control signal  $[(S_M)]$  if the absolute value  
43    $[(|\xi(n)|)]$  of said error signal at time  $n$  is smaller than the  
44   absolute value  $[(|\xi(n-1)|)]$  of the same error signal at time  $n-1$ ,  
45   maintaining otherwise unchanged the value of said control signal  
46    $[(S_{out})]$ .

1           2. (currently amended) The  $[[A]]$  method according to  
2 claim 1, wherein said step of accumulating said sign of said error  
3 signal  $[[\xi]]$  provides that the value accumulated has a positive  
4 saturation value of +4 and a negative saturation value of -4.

1           3. (currently amended) The  $[[A]]$  method according to  
2 claim 1, wherein said step of comparing said absolute value  
3  $[[(|\xi|)]]$  of said error signal  $[[\xi]]$  comprises:  $[-]$   
4           storing the absolute value  $[[(|\xi(n-1)|)]]$  of said error  
5 signal  $[[\xi]]$  in a first register  $[(72)]$ , maintaining such  
6 absolute value  $[[(|\xi(n-1)|)]]$  in said register  $[(72)]$  at least  
7 until a new absolute value  $[[(|\xi(n)|)]]$  of said error signal  $[[\xi]]$   
8 has been calculated;  $[-]$  and

9           comparing said new absolute value  $[[(|\xi(n)|)]]$  of said  
10 error signal  $[[\xi]]$  with the absolute value  $[[(|\xi(n-1)|)]]$  stored  
11 in said first register  $[(72)]$ , and storing said new absolute  
12 value  $[[(|\xi(n)|)]]$  in said first register  $[(72)]$ , overwriting the  
13 absolute value  $[[(|\xi(n-1)|)]]$  previously stored.

1           4. (currently amended) The  $[[A]]$  method according to  
2 claim 1, wherein said step of updating said control signal  
3  $[[S_{out}]]$  comprises:  $[-]$   
4           storing the value of a previous control signal  $[[S_{out}(n-$   
5  $1)]]$  in a second register  $[(78)]$ , maintaining such value in said

6 second register  $[(78)]$  at least until a new value of said  
7 intermediate control signal  $[(S_M)]$  has been calculated;  $[-]$  and  
8 overwriting the value of said control signal  $[(S_{out}(n))]$   
9 stored in said second register  $[(78)]$  with the new value of said  
10 intermediate control signal  $[(S_M)]$  if the absolute value  
11  $[(|\xi(n)|)]$  of said error signal at time  $n$  is smaller than the  
12 absolute value  $[(|\xi(n-1)|)]$  of the same error signal at time  $n-1$ ,  
13 maintaining otherwise unchanged the value stored in said second  
14 register  $[(78)]$ .

1 5. (currently amended) A digital communication receiver  
2 comprising a device for maintaining fine alignment between an  
3 incoming spread spectrum signal and a locally generated code, said  
4 device comprising:  $[-]$

5 a delay line  $[(56)]$  for storing a plurality of  
6 consecutive samples  $[(E-1, E, M, L, L+1)]$  of said incoming spread  
7 spectrum signal;  $[-]$

8 a first digitally controlled interpolator  $[(26)]$  for  
9 determining by interpolation between consecutive samples stored in  
10 said delay line  $[(56)]$  an interpolated early sample  $[(e)]$   
11 anticipating an optimal sampling time instant;  $[-]$

12 a second digitally controlled interpolator  $[(24)]$  for  
13 determining by interpolation between consecutive samples stored in  
14 said delay line  $[(56)]$  an interpolated middle sample  $[(m)]$   
15 corresponding to said optimal sampling time instant;  $[-]$

16 a third digitally controlled interpolator [(28)] for  
17 determining by interpolation between consecutive samples stored in  
18 said delay line [(56)] an interpolated late sample [(1)]  
19 delayed with respect to said optimal sampling time instant; [-]  
20 at least [a] one correlator [(30, 32, 22)] for  
21 calculating an error signal [( $\xi$ )] as the difference between the  
22 energy of the symbols computed from said interpolated early [(e)]  
23 and late [(1)] samples; [-] and  
24 a circuit for generating a control signal [(S<sub>out</sub>)] for  
25 controlling the interpolation phase of said second digitally  
26 controlled interpolator [(24)]; ~~characterised in that said~~  
27 wherein the means for generating a control signal [(S<sub>out</sub>)]  
28 comprises: [-]  
29 a circuit [(23)] for extracting the sign of said error  
30 signal [( $\xi$ )] ; [-]  
31 a circuit [(66)] for accumulating said sign of said  
32 error signal [( $\xi$ )] in a register, for the generation of an  
33 intermediate control signal [(S<sub>m</sub>)] ; [-]  
34 a circuit [(70)] for calculating the absolute value  
35 [(| $\xi(n)$ |)] of said error signal [( $\xi$ )] at a time instant n; [-]  
36 at least a comparator [(72, 74)] for comparing said  
37 absolute value [(| $\xi$ |)] of said error signal [( $\xi$ )] at said time  
38 instant n with the absolute value [(| $\xi(n-1)$ |)] of said error  
39 signal [( $\xi$ )] at a previous time instant n-1; [-] and

40 a controllable switch  $[(76, 78)]$  for updating said  
41 control signal  $[(S_{out})]$  to the value of said intermediate control  
42 signal  $[(S_M)]$  if the absolute value  $[(|\xi(n)|)]$  of said error  
43 signal at time  $n$  is smaller than the absolute value  $[(|\xi(n-1)|)]$   
44 of the same error signal at time  $n-1$ , maintaining otherwise  
45 unchanged the value of said control signal  $[(S_{out})]$ .

1 6. (currently amended) The  $[A]$  digital communication  
2 receiver according to claim 5, wherein said register in which is  
3 accumulated the sign of said error signal  $[(\xi)]$  has a positive  
4 saturation value of +4 and a negative saturation value of -4.

1 7. (currently amended) The  $[A]$  digital communication  
2 receiver according to claim 5, wherein said at least one comparator  
3  $[(72, 74)]$  for comparing said absolute value  $[(|\xi(n)|)]$  of said  
4 error signal  $[(\xi)]$  comprises:  $[-]$

5 a first register  $[(72)]$  for storing the absolute value  
6  $[(|\xi(n-1)|)]$  of said error signal  $[(\xi)]$  at a time instant  $n-1$ ,  
7 maintaining such absolute value  $[(|\xi(n-1)|)]$  in said register  
8  $[(72)]$  at least until a new absolute value  $[(|\xi(n)|)]$  of said  
9 error signal  $[(\xi)]$  has been calculated;  $[-]$  and

10 a comparator  $[(74)]$  for comparing said new absolute  
11 value  $[(|\xi|)]$  of said error signal  $[(\xi)]$  with the absolute value  
12  $[(|\xi(n-1)|)]$  stored in said first register  $[(72)]$ , generating a  
13 signal  $[(C_{out})]$  indicating whether said new absolute value

14      $[(|\xi(n)|)]$  is smaller than the previously stored absolute value  
15      $[(|\xi(n-1)|)]$ .

1             8. (currently amended) The  $[A]$  digital communication  
2 receiver according to claim 7, wherein said controllable switch  
3  $[(76, 78)]$  for updating said control signal  $[S_{out}]$  comprises:  
4  $[-]$

5             a second register  $[(78)]$  for storing the value of a  
6 previous control signal  $[S_{out}(n-1)]$ , maintaining such value in  
7 said register  $[(78)]$  at least until a new value of said  
8 intermediate control signal  $[S_M]$  has been calculated;  $[-]$  and

9             a switch  $[(76)]$ , controlled by the signal  $[C_{out}]$   
10 generated by said comparator  $[(74)]$ , for storing in said second  
11 register  $[(78)]$  a new value of said control signal  $[S_{out}(n)]$ ,  
12 if said new absolute value  $[(|\xi(n)|)]$  is smaller than the  
13 previously stored absolute value  $[(|\xi(n-1)|)]$ , or for leaving  
14 unaltered the value stored in the same register  $[(78)]$  if such  
15 condition is not verified.